Application No.: 10/065,646   Docket No.: JCLA9503

In the Claims

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) A code implantation process comprising:

forming a gate oxide layer on a surface of the substrate;

forming a plurality of conductive lines running in a first direction on the gate oxide layer, wherein the conductive lines are covered by a cap layer;

forming a dielectric layer over the substrate to cover the cap layer;

removing a portion of the dielectric layer until the cap layer is exposed;

forming a resist layer with a line/space pattern on the dielectric layer and the cap layer, wherein the line/space pattern extending in a second direction different from the first direction;

removing the cap layer not covered by the resist layer; and_

performing an ion implantation step to implant dopants into a region not covered by the cap layer.

2. (original) The process of claim 1, wherein the conductive lines and the cap layer have an etching selectivity.

3. (original) The process of claim 1, wherein the dielectric layer and the cap layer has an etching selectivity.

4. (original) The process of claim 1, wherein a material for forming the conductive lines includes polysilicon.

5. (original) The process of claim 1, wherein a material for forming the cap layer includes silicon oxide, while a material for forming the dielectric layer is silicon nitride or silicon oxynitride.

6. (original) The process of claim 1, wherein a material for forming the dielectric layer includes silicon oxide, while a material for forming the cap layer is silicon nitride or silicon oxynitride.

7. (original) The process of claim 1, wherein the first direction is perpendicular to the second direction.

8. (original) The process of claim 1, wherein a method for removing a portion of the dielectric layer until the cap layer being exposed is an etching back process or a CMP process.

9. (original) The process of claim 1, further comprising removing the resist layer before forming a code mask layer over the substrate.

10. (original) The process of claim 1, wherein a material for forming the code mask layer includes silicon oxide or resist.

11. (currently amended) A code implantation process for a mask read only memory (MROM), comprising:

forming a buried bitline in a substrate;

forming a gate oxide layer on a surface of the substrate;

forming a wordline on the gate oxide layer and forming a cap layer on a top of the wordline, wherein a stop layer is formed between the wordline and the cap layer;

forming a dielectric layer over the substrate to cover the cap layer;

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removing a portion of the dielectric layer until the cap layer is exposed;

forming a resist layer with a line/space pattern on the dielectric layer and the cap layer, wherein the line/space pattern has a first extending direction different to a second extending direction of the cap layer;

removing the cap layer not covered by the resist layer;

forming a code mask layer over the substrate; and_

performing an ion implantation step to implant dopants into a predetermined code channel region by using the code mask layer, the dielectric layer and the remained cap layer as a mask.

12. (original) The process of claim 11, wherein the stop layer and the cap layer have an etching selectivity.

13. (original) The process of claim 11, wherein the dielectric layer and the cap layer have an etching selectivity.

14. (original) The process of claim 11, wherein a material of the wordline is the same as that of the cap layer.

15. (original) The process of claim 11, wherein a material of the wordline is different to that of the cap layer.

16. (original) The process of claim 11, wherein a material for forming the wordline includes polysilicon.

17. (original) The process of claim 11, wherein a material of the cap layer includes polysilicon, while a material of the stop layer is silicon nitride or silicon oxynitride and a material of the dielectric layer is silicon oxide.

18. (original) The process of claim 11, wherein a material of the cap layer includes polysilicon, while a material of the stop layer is silicon oxide and a material of the dielectric layer is silicon nitride or silicon oxynitride.

19. (original) The process of claim 11, wherein the first extending direction of the line/space pattern is perpendicular to the second extending direction of the cap layer.

20. (original) The process of claim 11, wherein a method for removing a portion of the dielectric layer until the cap layer being exposed is an etching back process or a CMP process.

21. (original) The process of claim 11, further comprising removing the resist layer before forming a code mask layer over the substrate.

22. (original) The process of claim 11, wherein a material for forming the code layer includes silicon oxide or resist.

23. (original) The process of claim 11, wherein forming the wordline, the stop layer and the cap layer further comprises:

forming a conductive layer on the gate oxide layer;

forming an etching stop layer on the conductive layer;

forming a material layer on the etching stop layer; and

patterning the conductive layer, the etching stop layer and the material layer in a direction perpendicular to the buried bitline, to form the wordline, the stop layer and the cap layer on the top of the wordline.

Claims 24-28 (cancelled)